

Appl. No. 10/686,513
Amdt. dated June 7, 2007
Reply to Office Action of April 17, 2007

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REMARKS

Claims 36 to 117 were pending in the application at the time of examination. Claims 36 to 117 stand objected to under 37 C.F.R. 1.75. Claims 36 to 117 stand rejected as anticipated.

Prior to considering the rejections, Applicants respectfully note that a Revocation and Substitution of Power of Attorney has now been twice filed in the USPTO. Accordingly, the Examiner is respectfully requested to direct all further correspondence to Customer Number 24209.

Claims 36 to 117 stand objected to under 37 C.F.R. 1.75 as being substantial duplicates of Claims in U.S. Patent No. 7,107,581, and U.S. Patent No. 6,363,523.

Applicants note that while Paragraph 1 of the rejection quotes language concerning § 101 Double Patenting-same invention, the objection in Paragraph 2 of the rejection relies on 37 C.F.R. § 1.75 and MPEP § 706.03(k). Applicants respectfully traverse the objection of Claims 36 to 117.

The basis for the objection fails to support the objection

37 C.F.R. § 1.75 is directed at the requirements with respect to Claims in a single application and does not provide a basis for comparing claims in a pending application with a granted patent. Similarly, MPEP § 706.03(k) stated:

Inasmuch as a patent is supposed to be limited to only one invention or, at most, several closely related indivisible inventions, limiting an application to a single claim, or a single claim to each of the related inventions might appear to be logical as well as convenient. However, court decisions have confirmed applicant's right to restate (i.e., by plural claiming) the invention in a reasonable number of ways. Indeed, a mere difference in scope between claims has been held to be enough.

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Nevertheless, when two claims in an application are duplicates, or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other claim under 37 CFR 1.75 as being a substantial duplicate of the allowed claim. (Emphasis Added.)

The MPEP makes it clear that claims in a single application are being considered in both of the cited sections and not claims between an issued patent and a pending application. Therefore, the basis for the objection is not supported by the cited authorities. This alone is sufficient to overcome the rejection.

The Objection Eliminates Explicit Claim Limitations.

As described more completely below, the rejection eliminates a claim limitation from a Claim in the patent and then compares the new claim with the claims in the instant application. This is an incorrect form of analysis.

TABLE 1 is a Claim chart that compares Claim 36 in the instant application with Claim 1 in U.S. Patent No. 6,363,523. Limitations in Claim 1 in U.S. Patent No. 6,363,523 that are not found in Claim 36 are shown in bold.

TABLE 1

| Claim 36 Instant Application | Claim 1, U.S. Patent No. 6,363,523 |
|---|---|
| 36. (Previously Presented) A method for arithmetic expression optimization, comprising: | 1. A method for arithmetic expression optimization, comprising: |
| receiving a first instruction defined for a first processor | receiving a first instruction defined for a first processor |

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| having a first base, said instruction including an operator and at least one operand; and | having a first base, said instruction including an operator and at least one operand |
| converting said first instruction to a second instruction optimized for a second processor having a second base when said at least one operand does not carry potential overflow beyond said second base or when said operator is insensitive to overflow, said second base smaller than said first base | converting said first instruction to a second instruction optimized for a second processor having a second base when said at least one operand does not carry potential overflow beyond said second base or when said operator is insensitive to overflow, said second base smaller than said first base, and |
| | converting to a wider base a third instruction that is the source of potential overflow associated with said at least one operand when said at least one operand carries the potential for overflow beyond said second base and when said operator is sensitive to overflow, said third instruction having been previously optimized, said wider base larger than said second base and smaller or equal to said first base |

Claim 1 in U.S. Patent No. 6,363,523 includes multiple limitations. To recite the same invention, each of the

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multiple limitations must be found in the claims of the instant application. In particular, Claim 1 recites "converting to a wider base a third instruction." A process that does not perform such a conversion is not within the scope of Claim 1 in U.S. Patent No. 6,363,523. Claim 36 does not include such a converting operation. Therefore, the two claims are not directed at the same invention. Claim 1 in U.S. Patent No. 6,363,523 includes a limitation that is not in Claim 36. If the converting operation is removed, a different invention is obtained. The limitation defines which converting operation is within the scope of the claim and does not form a basis for eliminating the operation from the claim, as was done in the objection. Therefore, the two claims are not substantial duplicates and are not directed at the same invention.

There is no basis in anything cited in the objection for simply eliminating an explicit limitation from Claim 1 of the patent, as was done in the objection. When an explicit limitation is removed from the claim, a different claim is obtained by definition, which demonstrates that the objection has no merit. If the converting to a wider base operation is not done, Claim 1 in the patent is not applicable. Claims 56, 76, 96 are similar to Claim 36 and have the same differences as noted with respect to Claim 36 from corresponding structure Claims in U.S. Patent No. 6,363,523. Therefore, Applicants respectfully request reconsideration and withdrawal of the objection of each of Claims 36, 56, 76 and 96.

None of Claims 37 to 45 that depend from Claim 36 recite a "converting to a wider base a third instruction," while each of Claims 2 to 14 in U.S. Patent No. 6,363,523 depend from Claim 1 of the patent and include such a limitation. Therefore, each of Claims 37 to 45 is not a duplicate of any of claims 2 to 14 in U.S. Patent No. 6,363,523. Similarly, the claims dependent from Claims 56, 76 and 96 in the instant application are not duplicates of any claims in U.S. Patent No. 6,363,523 and

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Applicants request reconsideration and withdrawal of the objection to these dependent claims.

TABLE 2 is a Claim chart that compares Claim 46 in the instant application with Claim 1 in U.S. Patent No. 6,363,523. Limitations in Claim 1 in U.S. Patent No. 6,363,523 that are not found in Claim 46 are shown in bold.

TABLE 2

| Claim 46 Instant Application | Claim 1, U.S. Patent No. 6,363,523 |
|---|---|
| 46. (Previously Presented) A method for arithmetic expression optimization, comprising: | 1. A method for arithmetic expression optimization, comprising: |
| receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and | receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand |
| | converting said first instruction to a second instruction optimized for a second processor having a second base when said at least one operand does not carry potential overflow beyond said second base or when said operator is insensitive to overflow, said second base smaller than said first base; and |

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converting to a wider base a third instruction that is a source of potential overflow associated with said at least one operand when said at least one operand carries the potential for overflow beyond a second base of a second processor and when said operator is sensitive to overflow, said third instruction having been previously optimized, said second base smaller than said first base, said wider base larger than said second base and smaller or equal to said first base.

converting to a wider base a third instruction that is the source of potential overflow associated with said at least one operand when said at least one operand carries the potential for overflow beyond said second base and when said operator is sensitive to overflow, said third instruction having been previously optimized, said wider base larger than said second base and smaller or equal to said first base.

Claim 1 in U.S. Patent No. 6,363,523 includes multiple limitations. To recite the same invention, each of the multiple limitations must be found in the claims in the instant application. In particular, Claim 1 recites "converting said first instruction to a second instruction." A process that does not perform such a conversion is not within the scope of Claim 1 in U.S. Patent No. 6,363,523. Claim 46 does not include such a converting operation. Therefore, the two claims are not directed at the same invention. Claim 1 in U.S. Patent No. 6,363,523 includes a limitation that is not in Claim 46. If the converting operation is removed, a different invention is obtained. The limitation defines which converting operation is within the scope of the claim and does not form a basis for eliminating the operation from the claim, as was done in the

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objection. Therefore, the two claims are not substantial duplicates and are not directed at the same invention.

There is no basis in anything cited in the objection for simply eliminating an explicit limitation from a Claim as was done in the objection. When an explicit limitation is removed from the claim, a different claim is obtained by definition, which demonstrates that the objection has no merit. Claims 66, 86, and 106 are similar to Claim 46 and have the same differences as noted with respect to Claim 46 from corresponding structure Claims in U.S. Patent No. 6,363,523. Therefore, Applicants respectfully request reconsideration and withdrawal of the objection of each of Claims 46, 66, 86 and 106.

None of Claims 47 to 55 that depend from Claim 46 do recite "converting said first instruction to a second instruction," while each of Claims 2 to 14 in U.S. Patent No. 6,363,523 depend from Claim 1 of the patent and include such a limitation. Therefore, each of Claims 47 to 55 is not a duplicate of any of claims 2 to 14 in U.S. Patent No. 6,363,523. Similarly, the claims dependent from Claims 66, 86 and 96 in the instant application are not duplicates of any claims in U.S. Patent No. 6,363,523. Applicants request reconsideration and withdrawal of the objection to these dependent claims.

TABLE 3 is a Claim chart that compares Claim 116 in the instant application with Claim 35 in U.S. Patent No. 6,363,523. Limitations in Claim 35 in U.S. Patent No. 6,363,523 that are not found in Claim 116 are shown in bold.

TABLE 3

| | |
|-------------------------------|--|
| Claim 116 Instant Application | Claim 35, U.S. Patent No. 6,363,523 |
|-------------------------------|--|

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| 116. (Currently Amended) A smart card having a microcontroller embedded therein, the smart card comprising a virtual machine being executed by a microcontroller, the virtual machine executing a software application comprising of a plurality of previously optimized instructions, the instructions optimized by a method comprising: | 35. A smart card having a microcontroller embedded therein, the smart card comprising a virtual machine being executed by a microcontroller, the virtual machine executing a software application comprising of a plurality of previously optimized instructions, the instructions optimized by a method comprising: |
| receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and | receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; |
| converting said first instruction to a second instruction optimized for a second processor having a second base when said at least one operand does not carry potential overflow beyond said second base or when said operator is insensitive to overflow, said second base smaller than said first base; | converting said first instruction to a second instruction optimized for a second processor having a second base when said at least one operand does not carry potential overflow beyond said second base or when said operator is insensitive to overflow, said second base smaller than said first base; and |
| | converting to a wider base a third instruction that is the source of potential overflow |

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| | associated with said at least one operand when said at least one operand carries the potential for overflow beyond said second base and when said operator is sensitive to overflow, said third instruction having been previously optimized, said wider base larger than said second base and smaller or equal to said first base, |
| the virtual machine comprising: | the virtual machine comprising |
| means for receiving optimized instructions, the optimized instructions being previously optimized for execution on a resource-constrained device; and | means for receiving optimized instructions, the optimized instructions being previously optimized for execution on a resource-constrained device and |
| means for executing said instructions. | means for executing said instructions. |

Claim 35 in U.S. Patent No. 6,363,523 includes multiple limitations. To recite the same invention, each of the multiple limitations must be found in the claims of the instant application. In particular, Claim 35 recites "converting to a wider base a third instruction." A process that does not perform such a conversion is not within the scope of Claim 35 in U.S. Patent No. 6,363,523. Claim 116 does not include such a converting operation. Therefore, the two claims are not directed at the same invention. Claim 35 in U.S. Patent No. 6,363,523 includes a limitation that is not in Claim 116. The limitation defines which converting operation is within the

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scope of the claim and does not form a basis for eliminating the operation from the claim, as was done in the objection. Therefore, the two claims are not substantial duplicates and are not directed at the same invention.

There is no basis in anything cited in the objection for simply eliminating an explicit limitation from a Claim as was done in the objection. When an explicit limitation is removed from the claim, a different claim is obtained by definition, which demonstrates that the objection has no merit. Applicants respectfully request reconsideration and withdrawal of the objection of Claim 116.

TABLE 4 is a Claim chart that compares Claim 117 in the instant application with Claim 35 in U.S. Patent No. 6,363,523. Limitations in Claim 35 in U.S. Patent No. 6,363,523 that are not found in Claim 117 are shown in bold.

TABLE 4

| Claim 117 Instant Application | Claim 35, U.S. Patent No. 6,363,523 |
|---|--|
| 117. (Currently Amended) A smart card having a microcontroller embedded therein, the smart card comprising a virtual machine being executed by a microcontroller, the virtual machine executing a software application comprising of a plurality of previously optimized instructions, the instructions optimized by a method comprising: | 35. A smart card having a microcontroller embedded therein, the smart card comprising a virtual machine being executed by a microcontroller, the virtual machine executing a software application comprising of a plurality of previously optimized instructions, the instructions optimized by a method comprising: |

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| receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and | receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; |
| | converting said first instruction to a second instruction optimized for a second processor having a second base when said at least one operand does not carry potential overflow beyond said second base or when said operator is insensitive to overflow, said second base smaller than said first base; and |
| converting to a wider base a third instruction that is a source of potential overflow associated with said at least one operand when said at least one operand carries the potential for overflow beyond a second base of a second processor and when said operator is sensitive to overflow, said third instruction having been previously optimized, said second base smaller than said first base, said wider base larger than said second base | converting to a wider base a third instruction that is the source of potential overflow associated with said at least one operand when said at least one operand carries the potential for overflow beyond said second base and when said operator is sensitive to overflow, said third instruction having been previously optimized, said wider base larger than said second base and smaller or equal to said first base, |

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| | |
|---|--|
| and smaller or equal to said first base; | |
| the virtual machine comprising: | the virtual machine comprising |
| means for receiving optimized instructions, the optimized instructions being previously optimized for execution on a resource-constrained device; and | means for receiving optimized instructions, the optimized instructions being previously optimized for execution on a resource-constrained device and |
| means for executing said instructions. | means for executing said instructions. |

Claim 35 in U.S. Patent No. 6,363,523 includes multiple limitations. To recite the same invention, each of the multiple limitations must be found in the claims of the instant application. In particular, Claim 35 recites "converting said first instruction to a second instruction." A process that does not perform such a conversion is not within the scope of Claim 35 in U.S. Patent No. 6,363,523. Claim 117 does not include such a converting operation. Therefore, the two claims are not directed at the same invention. Claim 35 in U.S. Patent No. 6,363,523 includes a limitation that is not in Claim 117. The limitation defines which converting operation is within the scope of the claim and does not form a basis for eliminating the operation from the claim, as was done in the objection. Therefore, the two claims are not substantial duplicates and are not directed at the same invention.

There is no basis in anything cited in the objection for simply eliminating an explicit limitation from a Claim as was done in the objection. When an explicit limitation is removed from the claim, a different claim is obtained by definition, which demonstrates that the objection has no merit. Applicants

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respectfully request reconsideration and withdrawal of the objection of Claim 117.

TABLE 5 is a Claim chart that compares Claim 36 in the instant application with Claim 1 in U.S. Patent No. 7,107,581. Differences in Claim 1 in U.S. Patent No. 7,107,581 with Claim 36 are shown in bold in Claim 1. Differences in Claim 36 and Claim 1 of U.S. Patent No. 7,107,581 are shown by underline in Claim 36.

TABLE 5

| Claim 36 Instant Application | Claim 1, U.S. Patent No. 7,107,581 |
|---|--|
| 36. (Previously Presented) A method for arithmetic expression optimization, comprising: | 1. A method for arithmetic expression optimization, comprising: |
| receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and | receiving a first instruction defined for a first processor having a first base, said instruction comprising an operator and at least one operand having an operand type; |
| converting said first instruction to a second instruction optimized for a second processor having a second base <u>when said at least one operand does not carry potential overflow beyond said second base or when said operator is insensitive to</u> | converting said first instruction to a second instruction optimized for a second processor having a second base when overflow is not possible based at least in part on said operator and the relationship between said operand type and said second |

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| overflow, said second base smaller than said first base | base, said second base smaller than said first base |
|--|--|
| | converting instructions in a chain of instructions to a wider base when said at least one operand carries the potential for overflow beyond said second base and when said operator is sensitive to overflow, said chain bounded by said second instruction and a third instruction that is the source of potential overflow associated with said at least one operand, said third instruction having been previously optimized, said wider base larger than said second base and smaller or equal to said first base. |

Claim 1 in U.S. Patent No. 7,107,581 includes multiple limitations. To recite the same invention, each of the multiple limitations must be found in the claims of the instant application. In particular, Claim 1 recites "converting instructions in a chain of instructions to a wider base." A process that does not perform such a conversion is not within the scope of Claim 1 in U.S. Patent No. 7,107,581. Claim 36 does not include such a converting operation. Therefore, the two claims are not directed at the same invention. Claim 1 in U.S. Patent No. 7,107,581 includes a limitation that is not in Claim 36. The limitation defines which converting operation is within the scope of the claim and does not form a basis for eliminating the operation from the claim, as was done in the

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objection. Therefore, the two claims are not substantial duplicates and are not directed at the same invention.

There is no basis in anything cited in the objection for simply eliminating an explicit limitation from a Claim as was done in the objection. When an explicit limitation is removed from the claim, a different claim is obtained by definition, which demonstrates that the objection has no merit. Claims 56, 76, 96 are similar to Claim 36 and have the same differences as noted with respect to Claim 36 from corresponding structure Claims in U.S. Patent No. 7,107,581. Therefore, Applicants respectfully request reconsideration and withdrawal of the objection of each of Claims 36, 56, 76 and 96.

None of Claims 37 to 45 that depend from Claim 36 recite a converting instructions in a chain of instructions to a wider base," while each of Claims 2 to 13 in U.S. Patent No. 7,107,581 depend from Claim 1 of the patent and include such a limitation. Therefore, each of Claims 37 to 45 is not a duplicate of any of claims 2 to 13 in U.S. Patent No. 7,107,581. Similarly, the claims dependent from Claims 56, 76 and 96 in the instant application are not duplicates of any claims in U.S. Patent No. 7,107,581 and Applicants request reconsideration and withdrawal of the objection to these dependent claims.

TABLE 6 is a Claim chart that compares Claim 46 in the instant application with Claim 1 in U.S. Patent No. 7,107,581. Differences in Claim 1 in U.S. Patent No. 7,107,581 with Claim 46 are shown in bold in Claim 1.

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TABLE 6

| Claim 46 Instant Application | Claim 1, U.S. Patent No. 7,107,581 |
|--|--|
| 46. (Previously Presented) A method for arithmetic expression optimization, comprising: | 1. A method for arithmetic expression optimization, comprising: |
| receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and | receiving a first instruction defined for a first processor having a first base, said instruction comprising an operator and at least one operand having an operand type; |
| | converting said first instruction to a second instruction optimized for a second processor having a second base when overflow is not possible based at least in part on said operator and the relationship between said operand type and said second base, said second base smaller than said first base |
| converting to a wider base a third instruction that is a source of potential overflow associated with said at least one operand when said at least one operand carries the potential for overflow beyond a second base of a second | converting instructions in a chain of instructions to a wider base when said at least one operand carries the potential for overflow beyond said second base and when said operator is sensitive to overflow, said chain bounded |

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processor and when said operator is sensitive to overflow, said third instruction having been previously optimized, said second base smaller than said first base, said wider base larger than said second base and smaller or equal to said first base.

by said second instruction and a third instruction that is the source of potential overflow associated with said at least one operand, said third instruction having been previously optimized, said wider base larger than said second base and smaller or equal to said first base.

Claim 1 in U.S. Patent No. 7,107,581 includes multiple limitations. To recite the same invention, each of the multiple limitations must be found in the claims of the instant application. In particular, Claim 1 recites "converting said first instruction to a second instruction." A process that does not perform such a conversion is not within the scope of Claim 1 in U.S. Patent No. 7,107,581. However, Claim 46 does not include such a converting operation. Therefore, the two claims are not directed at the same invention. Claim 1 in U.S. Patent No. 7,107,581 includes a limitation that is not in Claim 46. The limitation defines which converting operation is within the scope of the claim and does not form a basis for eliminating the operation from the claim, as was done in the objection. Therefore, the two claims are not substantial duplicates and are not directed at the same invention.

There is no basis in anything cited in the objection for simply eliminating an explicit limitation from a Claim as was done in the objection. When an explicit limitation is removed from the claim, a different claim is obtained by definition, which demonstrates that the objection has no merit. Claims 66, 86, and 106 are similar to Claim 46 and have the same differences as noted with respect to Claim 46 from corresponding structure Claims in U.S. Patent No. 7,107,581.

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Therefore, Applicants respectfully request reconsideration and withdrawal of the objection of each of Claims 46, 66, 86 and 106.

None of Claims 47 to 55 that depend from Claim 46 do recite "converting said first instruction to a second instruction," while each of Claims 2 to 13 in U.S. Patent No. 7,107,581 depend from Claim 1 of the patent and include such a limitation. Therefore, each of Claims 47 to 55 is not a duplicate of any of claims 2 to 13 in U.S. Patent No. 7,107,581. Similarly, the claims dependent from Claims 66, 86 and 96 in the instant application are not duplicates of any claims in U.S. Patent No. 7,107,581. Applicants request reconsideration and withdrawal of the objection to these dependent claims.

TABLE 7 is a Claim chart that compares Claim 116 in the instant application with Claim 54 in U.S. Patent No. 7,107,581.

Differences in Claim 54 in U.S. Patent No. 7,107,581 with Claim 116 are shown in bold in Claim 54. Differences in Claim 116 and Claim 54 of U.S. Patent No. 7,107,581 are shown by underline in Claim 116.

TABLE 7

| Claim 116 Instant Application | Claim 54, U.S. Patent No. 7,107,581 |
|--|---|
| 116. (Currently Amended) A smart card having a microcontroller embedded therein, the smart card comprising a virtual machine being executed by a microcontroller, the virtual machine executing a software | 54. A smart card having a microcontroller embedded therein, said microcontroller configured to execute a virtual machine, the virtual machine capable of executing a software application comprising a plurality of |

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| application comprising of a plurality of previously optimized instructions, the instructions optimized by a method comprising: | previously optimized instructions, the instructions optimized by a method comprising: |
| | receiving the software program on said processor, said software program optimized according to a method comprising: |
| receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and | receiving a first instruction defined for a first processor having a first base, said instruction comprising an operator and at least one operand having an operand type; |
| converting said first instruction to a second instruction optimized for a second processor having a second base <u>when said at least one operand does not carry potential overflow beyond said second base or when said operator is insensitive to overflow</u> , said second base smaller than said first base; | converting said first instruction to a second instruction optimized for a second processor having a second base when overflow is not possible based at least in part on said operator and the relationship between said operand type and said second base, said second base smaller than said first base; and |
| | converting instructions in a chain of instructions to a wider base when said at least one operand carries the potential for overflow beyond said second base and when said |

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| | operator is sensitive to overflow, said chain bounded by said second instruction and a third instruction that is the source of potential overflow associated with said at least one operand, said third instruction having been previously optimized, said wider base larger than said second base and smaller or equal to said first base. |
| <u>the virtual machine comprising:</u> | |
| <u>means for receiving optimized instructions, the optimized instructions being previously optimized for execution on a resource-constrained device;</u> | |
| <u>and</u> | |
| <u>means for executing said instructions.</u> | |

Claim 54 in U.S. Patent No. 7,107,581 includes multiple limitations. To recite the same invention, each of the multiple limitations must be found in the claims of the instant application. In particular, Claim 54 recites "converting instructions in a chain of instructions to a wider base." A process that does not perform such a conversion is not within the scope of Claim 54 in U.S. Patent No. 7,107,581. Claim 116 does not include such a converting operation. Therefore, the two claims are not directed at the same invention. Claim 54 in U.S. Patent No. 7,107,581 includes a limitation that is not in Claim 116. The limitation defines which converting operation

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is within the scope of the claim and does not form a basis for eliminating the operation from the claim, as was done in the objection. Therefore, the two claims are not substantial duplicates and are not directed at the same invention.

There is no basis in anything cited in the objection for simply eliminating an explicit limitation from a Claim as was done in the objection. When an explicit limitation is removed from the claim, a different claim is obtained by definition, which demonstrates that the objection has no merit. Applicants respectfully request reconsideration and withdrawal of the objection of Claim 116.

TABLE 8 is a Claim chart that compares Claim 117 in the instant application with Claim 54 in U.S. Patent No. 7,107,581. Differences in Claim 54 in U.S. Patent No. 7,107,581 with Claim 117 are shown in bold in Claim 54.

TABLE 8

| Claim 117 Instant Application | Claim 54, U.S. Patent No. 7,107,581 |
|---|---|
| 117. (Currently Amended) A smart card having a microcontroller embedded therein, the smart card comprising a virtual machine being executed by a microcontroller, the virtual machine executing a software application comprising of a plurality of previously optimized instructions, the instructions optimized by a method comprising: | 54. A smart card having a microcontroller embedded therein, said microcontroller configured to execute a virtual machine, the virtual machine capable of executing a software application comprising a plurality of previously optimized instructions, the instructions optimized by a method comprising: |

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| | receiving the software program on said processor, said software program optimized according to a method comprising: |
| receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and | receiving a first instruction defined for a first processor having a first base, said instruction comprising an operator and at least one operand having an operand type; |
| | converting said first instruction to a second instruction optimized for a second processor having a second base when overflow is not possible based at least in part on said operator and the relationship between said operand type and said second base, said second base smaller than said first base; and |
| converting to a wider base a third instruction that is a source of potential overflow associated with said at least one operand when said at least one operand carries the potential for overflow beyond a second base of a second processor and when said operator is sensitive to overflow, said third | converting instructions in a chain of instructions to a wider base when said at least one operand carries the potential for overflow beyond said second base and when said operator is sensitive to overflow, said chain bounded by said second instruction and a third instruction that is the source of potential |

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| instruction having been previously optimized, said second base smaller than said first base, said wider base larger than said second base and smaller or equal to said first base; | overflow associated with said at least one operand, said third instruction having been previously optimized, said wider base larger than said second base and smaller or equal to said first base. |
| the virtual machine comprising: | |
| <u>means for receiving optimized instructions, the optimized instructions being previously optimized for execution on a resource-constrained device;</u> | |
| and | |
| <u>means for executing said instructions.</u> | |

Claim 54 in U.S. Patent No. 7,107,581 includes multiple limitations. To recite the same invention, each of the multiple limitations must be found in the claims of the instant application. In particular, Claim 54 recites "converting said first instruction to a second instruction." A process that does not perform such a conversion is not within the scope of Claim 54 in U.S. Patent No. 7,107,581. However, Claim 117 does not include such a converting operation. Therefore, the two claims are not directed at the same invention. Claim 54 in U.S. Patent No. 7,107,581 includes a limitation that is not in Claim 117. The limitation defines which converting operation is within the scope of the claim and does not form a basis for eliminating the operation from the claim, as was done in the objection. Therefore, the two claims are not substantial duplicates and are not directed at the same invention.

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There is no basis in anything cited in the objection for simply eliminating an explicit limitation from a Claim as was done in the objection. When an explicit limitation is removed from the claim, a different claim is obtained by definition, which demonstrates that the objection has no merit. Therefore, Applicants respectfully request reconsideration and withdrawal of the objection to Claim 117.

The 102(e) rejection has no support.

Claims 36 to 117 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,363,523. Applicants respectfully traverse the anticipation of Claims 36 to 117.

U.S. Patent No. 6,363,523 was filed in the name of inventors, Zhiqun Chen and Judith E. Schwabe, on November 12, 1999. The instant application was filed in the name of inventors Zhiqun Chen and Judith E. Schwab. A copy of the declaration filed with respect to U.S. Patent No. 6,363,523 was filed in the instant application. Thus, the inventive entity in the instant application and U.S. Patent No. 6,363,523 are the same entity. Therefore, the invention in the instant application is not "of another" and so § 102(e) is not applicable.

The lack of a proper entity for the § 102(e) rejection was previously pointed out and was not addressed in the final rejection. Rather, a statement about "the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000," was cited. Neither the instant application nor U.S. Patent No. 6,363,523 resulted directly or indirectly from an International Application. Therefore, the rejection has relied upon material that is not applicable.

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The reference date for U.S. Patent No. 6,363,523 is the earliest U.S. filing date November 12, 1999. There is no international application involved.

To determine whether the date of the reference is before the earliest date of invention, as required by 102(e) the effective filing date of the instant application must be determined. The effective filing date is the earliest date of invention based only on the pending record.

The MPEP directs:

V.DETERMINING THE EFFECTIVE FILING DATE OF THE APPLICATION

The effective filing date of a U.S. application may be determined as follows:

(A) If the application is a continuation or divisional of one or more earlier U.S. applications or international applications and if the requirements of 35 U.S.C. 120 and 365(c), respectively, have been satisfied, the effective filing date is the same as the earliest filing date in the line of continuation or divisional applications.

MPEP 706.02, 8th Ed., Rev. 5, pg. 700-23 (August 2006).

The instant application was filed on October 14, 2003 and is a continuation of U.S. Patent Application Serial No. 10/002,437, entitled "Optimization Of N-Base Typed Arithmetic Expressions," by Zhiqun Chen and Judy Schwabe, filed on November 1, 2001. U.S. Patent Application Serial No. 10/002,437 issued as U.S. Patent No. 6,687,898 B2 on February 3, 2004. Accordingly, the instant application and U.S. Patent Application Serial No. 10/002,437 were copending.

U.S. Patent Application Serial No. 10/002,437 was a continuation of U.S. Patent Application No. 09/439,113 that issued as U.S. Patent 6,363,523 on March 26, 2002. Therefore, these applications were also copending.

Thus, there is a chain of continuity between the instant application and U.S. Patent Application No. 09/439,113 that issued as U.S. Patent 6,363,523. Therefore, the instant

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application is entitled to the filing date of November 12, 1999, the earliest filing date in the line of continuations, according to the MPEP. Accordingly, the date of invention for the instant application is at least November 12, 1999.

35 U.S.C. § 102(e) requires:


(e) the invention was described in - (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent

Applicants have demonstrated that the application for patent was not "by another," and that the date of the reference was not "before the invention by applicant." Therefore, the § 102(e) rejection is without merit. Applicants respectfully request reconsideration and withdrawal of the anticipation rejection of Claims 36 to 117.

Claims 36 to 117 remain in the application. For the foregoing reasons, Applicants respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicants.

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the U.S. Patent and Trademark Office, Fax No. (571) 273-8300, on June 7, 2007.


Amanda Ream

June 7, 2007
Date of Signature

Respectfully submitted,



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